PAN ARCHIVES OF ACOUSTICS
Vol. 41, No. 4, pp. 773–781 (2016)

DOI: 10.1515/aoa-2016-0074

Research and Medical Transcranial Doppler System

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(*received March 28, 2016; accepted September 21, 2016*)

A new ultrasound digital transcranial Doppler system (digiTDS) is introduced. The digiTDS enables diagnosis of intracranial vessels which are rather difficult to penetrate for standard systems. The device can display a color map of flow velocities (in time-depth domain) and a spectrogram of a Doppler signal obtained at particular depth. The system offers a multigate processing which allows to display a number of spectrograms simultaneously and to reconstruct a flow velocity profile.

The digital signal processing in digiTDS is partitioned between hardware and software parts. The hardware part (based on FPGA) executes a signal demodulation and reduces data stream. The software part (PC) performs the Doppler processing and display tasks. The hardware-software partitioning allowed to build a flexible Doppler platform at a relatively low cost.

The digiTDS design fulfills all necessary medical standards being a new useful tool in the transcranial field as well as in heart velocimetry research.

Keywords: Doppler system; digital signal processing; hardware-software partitioning; field programmable gate arrays.

1. Introduction

Ultrasound Doppler techniques are diagnostic tools which are implemented in a quickly growing number of devices. However, due to specific conditions of transcranial examinations most of the devices offer results of poor quality. Only a few systems are dedicated to the transcranial diagnosis.

RIMED Digi-Lite (RIMED, Israel) is a dual channel TCD (Transcranial Doppler) system with an advanced and proprietary M-Mode Display. The system has a complete range of probes including 2 MHz, 4 MHz, 8 MHz, and 16 MHz, each with a separate connector. The 2 MHz probe can insonify the brain in 64 different depths/gates at the same time, displaying 8 different Doppler spectrum windows simultaneously. Its high sensitivity enables detection of flow velocity at the contra-lateral side of the brain. It offers an optional imaging probe for complete and accurate colour-coded ultrasound scanning of the Carotid System.

SONARA TCD System (SONARA, USA) allows TCD exams to be performed quickly and more efficiently utilising M-Mode which includes 250 gates/depths. The system is available in unilateral and bilateral configuration and gives access to patient files in multiple export formats including raw data.

DWL Multi-Dop X Digital (Compumedics, Germany) is a dual channel Doppler system with 400 gates of M-Mode display and 4 spectrum windows. It can operate both in pulsed and continuous wave modes in the frequency range of 1 to 16 MHz and gives access to raw data.

The model example of combined ultrasound system architecture is a Doppler device introduced in (Fan *et al.*, 2006; Ricci *et al.*, 2008). The basic design of their system is similar to that of digiTDS. The module designed by Ricci *et al.* is composed of FPGA (Altera® Stratix) executing hardware processing functions, and DSP (Texas Instruments® TMS320C67). The module communicates with a PC and is responsible for the control and display functions through the

USB interface. The quadrature demodulator, a set of digital filters and a decimator have been implemented in FPGA. The initially demodulated and decimated data stream is transferred to the DSP that executes standard Doppler algorithms. Although the reported system is not a commercial solution, its construction is similar to that of the devices offered on the market.

Both systems are based on a mixed model of hardware-software signal processing (Bassam *et al.*, 2009; Reed, 2002). The acquisition of the RF echo signal is based on a fast A/D converter and FPGA – an interface to the further part of the system. The application of FPGA at the beginning of the digital channels is now a standard solution. Apart from signal acquisition, the FPGA most often executes hardware processing of a digital signal, the aim of which is to reduce the data stream for further processing (Garcia *et al.*, 2006). Next, the processing is executed by DSP, GPP, GPU, or combinations of these processors (Chang *et al.*, 2009).

2. Transcranial Doppler System – digiTDS

The pulse wave Doppler method is a standard for intracranial diagnostic device allowing to measure the flow at a selected depth. The current diagnostic solutions are mainly focused on complex assessment and monitoring of cerebrovascular flow in various pathological conditions, especially those potentially affecting normal function of the central nervous system. The digiTDS device (Fig. 1) is a multigate transcranial Doppler system (Lewandowski *et al.*, 2009).

Fig. 1. Photo of the complete digiTDS system.

This system is composed of two electronic modules of 130×82 mm dimensions (Fig. 2), responsible for high frequency signal transmission, acquisition and demodulation, and the PC responsible for Doppler signal processing after demodulation and for data presentation. Figure 3 shows the system block scheme. On an analogue-digital module board, there are two independent transmission-reception channels (the device supports simultaneous operation with two probes

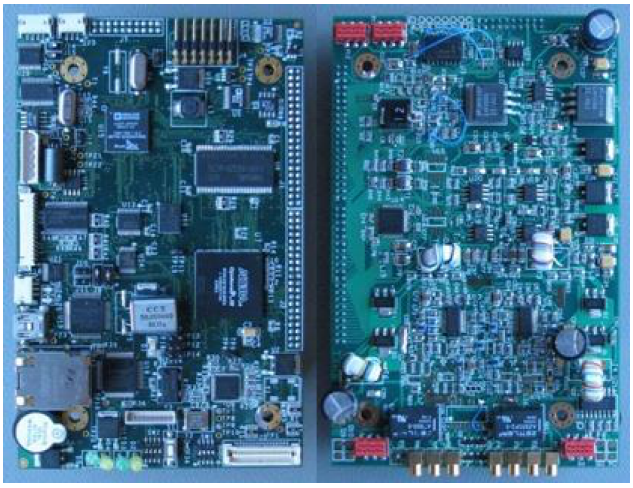

Fig. 2. Photos of the digiTDS's electronic modules: digital module (left), mixed-signal module (right).

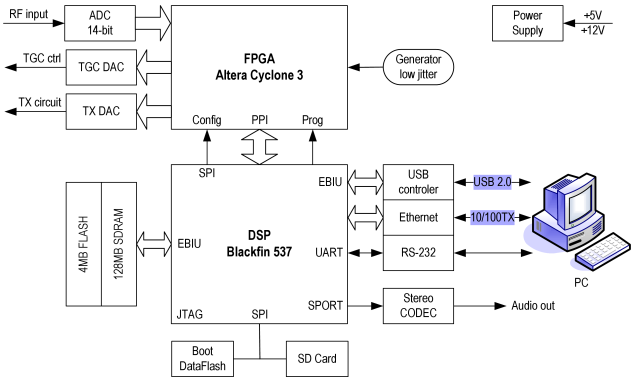

Fig. 3. Simplified block diagram of the digiTDS system.

in bilateral operation mode). A 10-bit DAC (Texas Instruments® DAC5652A) operating at a speed of 64 MSPS is used to generate the transmitted signal. The reception track contains amplifiers including time gain compensation TGC (Analogue Devices® AD8331) and a dual 14-bit ADC (Analogue Devices® AD9640) with sampling frequency of 64 MHz. The digital signals from ADC are connected to FPGA on the digital module board via inter module connector. The digital module consists of FPGA (Altera® Cyclone 3 EP3C25), DSP (Analog Devices® Blackfin BF537), as well as USB device controller (PLX® NET2272) and an Ethernet interface. The digiTDS communicates with PC via USB 2.0 interface. However, it can run independently of PC, thanks to its own control resources – DSP processor.

3. Digital signal processing

The digital processing chain consists of hardware processing in the FPGA and software processing using DSP and PC's CPU. The application of hardware resources during early processing stage allowed to significantly decrease the required data throughput and

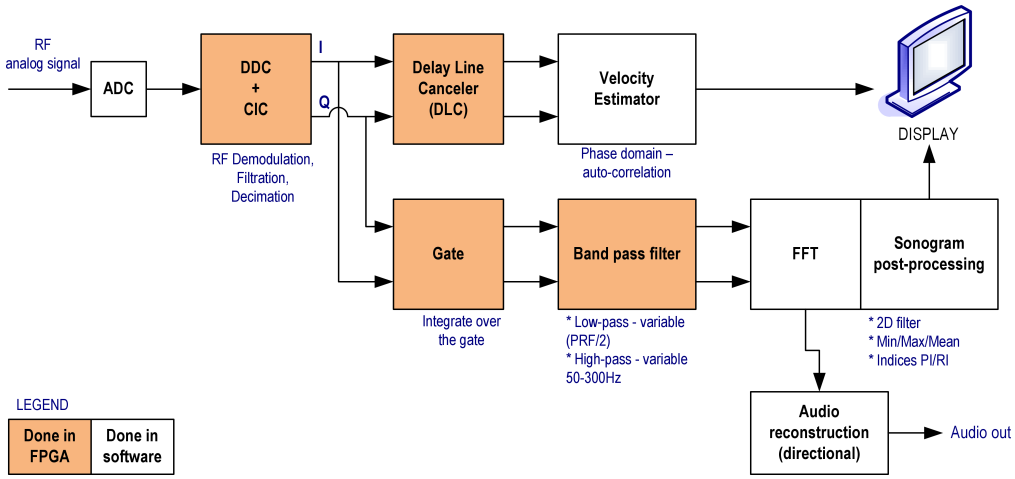

Fig. 4. Doppler digital signal processing chain.

computing load of PC (Martinez-Nieto *et al.*, 2009). It also allowed to use a low-power single-board PC with Intel® ATOM processor and to extend the operating time on batteries. The distribution and implementation of processing tasks were performed and tested on a constructed prototype device. Especially, moving the realisation of filtration in multiple gates from software to the FPGA enabled a significant processor time saving. Figure 4 presents the track of Doppler digital signal processing on the digiTDS device with task distribution between the FPGA system and the software.

3.1. Preprocessing – FPGA

The data path of the implemented FPGA logic (Fig. 5) consists of three components: a quadrature demodulator (DDC – Digital Down Converter), a decimator (integrated into a CIC filter – Cascaded Integrator Comb), and a set of wall filters.

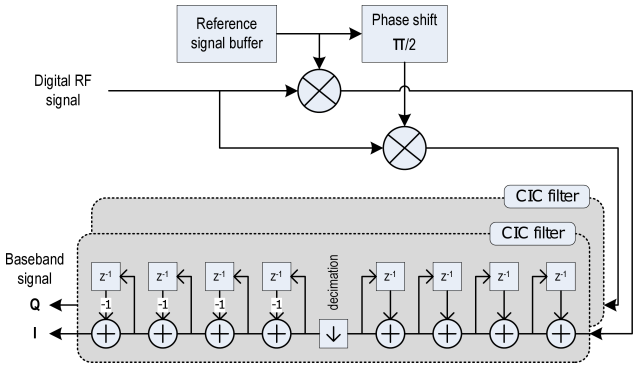

Fig. 5. Block diagram of the digital quadrature demodulator with CIC filter implemented in the FPGA.

The DDC employs a quadratic demodulation to convert the received radio frequency real signal (RF) to a complex signal (I/Q – in phase/quadrature) centered at zero frequency baseband (0 Hz to a few kHz). Thus, it allows to decrease the sampling frequency – there is no need to sample the signal of a few kHz with a frequency of 64 MHz. Moreover, the resulting quadrature I/Q signal enables to easily separate flow directions in further processing.

The DDC accepts 14-bit RF echo signal samples in two's complement format at its input port and produces a pair of 28-bit down-converted I/Q signals at its output ports. The demodulator is composed of two multipliers, six memories containing reference signals, and two multiplexers. Each of the memories contains one period of reference sine and cosine signals sampled at 64 MHz with 14-bit resolution.

The two multipliers were implemented as Altera IP *lpm_mult* components. The first port of the multipliers is directly connected to the input port of the demodulator, the second is connected via 3-to-1 multiplexer to the memory containing reference signal samples. It gives a choice of selecting one of three demodulation frequencies. Output ports of the multipliers are directly connected to the output ports of the demodulator.

The I/Q signal is next passed on to a CIC (Hogenauer, 1981; Lyons, 2004) (Cascaded Integrator Comb) filter which is an efficient finite impulse response, low-pass filter dedicated for decimation. It performs both anti-aliasing filtration and decimation. In comparison to standard FIR filters it offers frequency response (Fig. 6) which is well matched for decimation purposes for relatively low computation cost (Harris, 2004).

Each CIC filter accepts 28-bit down-converted RF echo signal samples at its input port and produces 35-bit decimated baseband signal at its output port. The CIC filter is composed of a recursive integrator, a decimator, and a differentiator. The decimation factor is run-time programmable, thus it enables controlling the Doppler gate size as well as raw data throughput (increasing the decimation factor decreases the

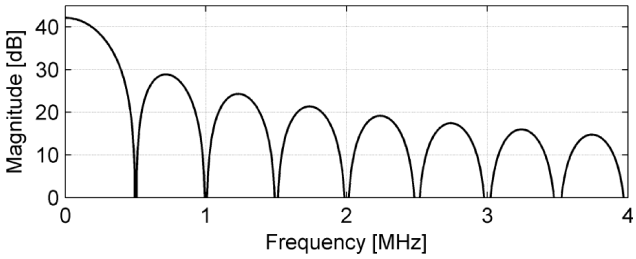

Fig. 6. Impulse response of the CIC filter for the decimation factor set to 128. The sampling frequency is 64 MHz. The CIC filter prepares the signal for a decimation which involves spectral folding. The zeros of the filter's frequency response are related to the frequencies which would alias directly into the desired baseband.

data rate and increases the effective Doppler gate size). In a typical transcranial operation mode the decimation factor is set to 128, which sets the Doppler gate size to 2 μs (1.5 mm) and reduces the data rate from 64 MSPS to 0.5 MSPS.

The two 35-bit output ports of the CIC filters are connected to the 16-bit input ports of the wall filter component via a Gain and Saturation block. The role of the Gain and Saturation block is to select which 16 of 35 bits of the output port of the CIC filter are connected to the input port of the wall filter.

The wall filter is a high-pass filter which is intended to suppress low-frequency signals related to a stationary tissue (e.g. vessel's walls – hence the name). The wall filter implemented in the FPGA performs an initial filtration only. It allows to reduce complexity of the final wall filters which are implemented in PC/DSP.

The choice of the wall filter's structure was made with respect to various aspects. An IIR structure offers good frequency response for low computation costs. However, when fed with input signals of higher amplitude, it becomes unstable. Employment of IIR filter would force to limit the input signal's dynamic range, which is highly undesirable. Finally a FIR filter type was chosen due to its unconditioned stability. Figure 7 presents a frequency response of an exemplary initial wall filter implemented in the digiTDS.

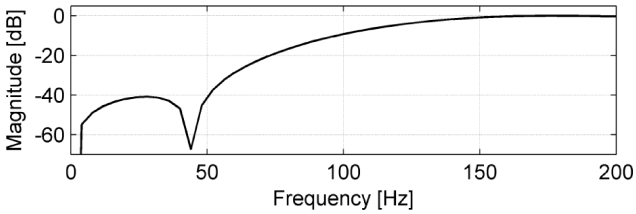

Fig. 7. Exemplary impulse response of the initial wall filter. The filter is implemented as a 64-taps FIR filter. The sampling frequency is 4 kHz.

From the functional viewpoint the wall filter component is composed of 200 FIR filters (two for each of 100 gates, one for I and one for Q data), each with the length of 64 run-time programmable coefficients. This filter bank operates in a fully serial manner, which means that it performs one multiply-accumulate operation per clock cycle and it takes 64 clock cycles to filter one Doppler gate.

From the structural viewpoint the wall filter is composed of a memory bank containing FIR filter states, a memory containing FIR filter coefficients, two multipliers, and two accumulators. In order to use the FPGA memory resources optimally, the memory bank containing the FIR filter states was implemented as 25 Altera IP *altsyncram* components each in a 256 words by 32 bits configuration, and the memory containing FIR filer coefficients was implemented as a single *altsyncram* component in a 64 words by 16 bits configuration. Multipliers were implemented as 16-bit Altera IP *lpm_mult* components, whereas accumulators were implemented as 38-bit Altera IP *altaccumulate* components. They perform together a single multiply-accumulate operation, separate for the I and Q channels. The wall filter output ports are connected to the final data path multiplexer via Gain and Saturation blocks. The role of the Gain and Saturation blocks is to select 16 of 38 bits of the wall filter output port for further software processing.

The cumulative utilisation of logical resources of the applied FPGA (Altera® EP3C25) amounted to 43% of logic cells, 79% of internal block RAM, and 12% of dedicated 18-bit multipliers. Time closure was obtained for the frequency of 64 MHz, and thus the processing speed matched the speed of input data stream (RF signal sampling).

Afterwards the processed signal is sent to PC where it is processed specifically for a given application including colour flow M-mode (Color) and Doppler spectral analysis (Spectrum). The Color mode display allows the operator to easily find a preferred blood vessel and apply the Spectrum mode which enables a more complete analysis of the flow vascular conditions.

3.2. Color channel

The processing in the Colour channel starts with a final wall filter which removes the residual remains of clutter echoes after the initial wall filtration executed in the FPGA. A mean frequency estimation which follows the filtration, is heavily sensitive to low frequency clutters. Thus, additional rejection of the clutter is crucial for the whole Colour chain to work correctly (Ali, 2008; Bjaerum, Torp, 2000).

The choice of the wall filter type was made with respect to the quality of the frequency estimation (Kadi, Loupas, 1995). The computational simplicity was important as well since the filtration needs to be performed for all 100 gates simultaneously. Based on simulations and experiments with different filter implementations on the prototype device we decided to choose

a linear regression filter. A frequency response of the filter is shown in Fig. 8.

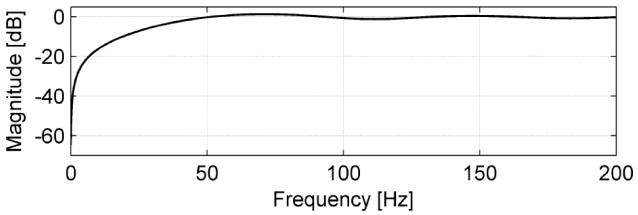

Fig. 8. Exemplary impulse response of the final wall filter in the Colour chain. The filter is implemented as a linear regression filter with the window length of 59 samples. The sampling frequency is 4 kHz.

The slope of the employed filter is 6dB/octave and the cut-off frequency depends on the filter's window length. As the initial wall filter (FIR) is adjusted to the standard conditions of the Doppler examination, the regression filter is intended only to efficiently suppress the clutter of the lowest frequency and the highest amplitude. Thus, in the digiTDS the regression filter's cut-off frequency is set to relatively low frequencies varying from 27 Hz to 110 Hz (variety of cut-off frequencies results from implementation reasons rather than signal processing).

The signal is next passed to the autocorrelation-based mean frequency estimator (Yu *et al.*, 2007). The results depend on time and depth thus can be used to form a 2D map of Doppler frequencies (Fig. 9e).

However, such a map not only pictures the flow of blood but also contains a random noisy background which has to be eliminated. To reject the unwanted part of the map of frequencies we use an adaptive background rejection algorithm which employs a map of autocorrelation (AC) factor values (Fig. 9a). This map is generated in the process of mean frequency estimation, so no additional computations are required. The autocorrelation factor behaves similarly to the Doppler power factor.

In fact, the power is commonly used for the background rejection. However, we observed that the autocorrelation factor allows the adaptive background rejection algorithm to perform more efficiently, so it is the next part of the Colour chain for improved performance.

The background rejection algorithm analyses the histogram (Fig. 9c) of the autocorrelation map to estimate the threshold of acceptable autocorrelation factor values. The histogram usually contains two partially overlapping gaussian distributions which represent stationary tissue (lower values of AC factor) and moving blood (higher values of AC factor). The algorithm searches for a minimum value of the histogram between maxima of both distributions. The argument of this minimum is the threshold level of the autocorrelation factor.

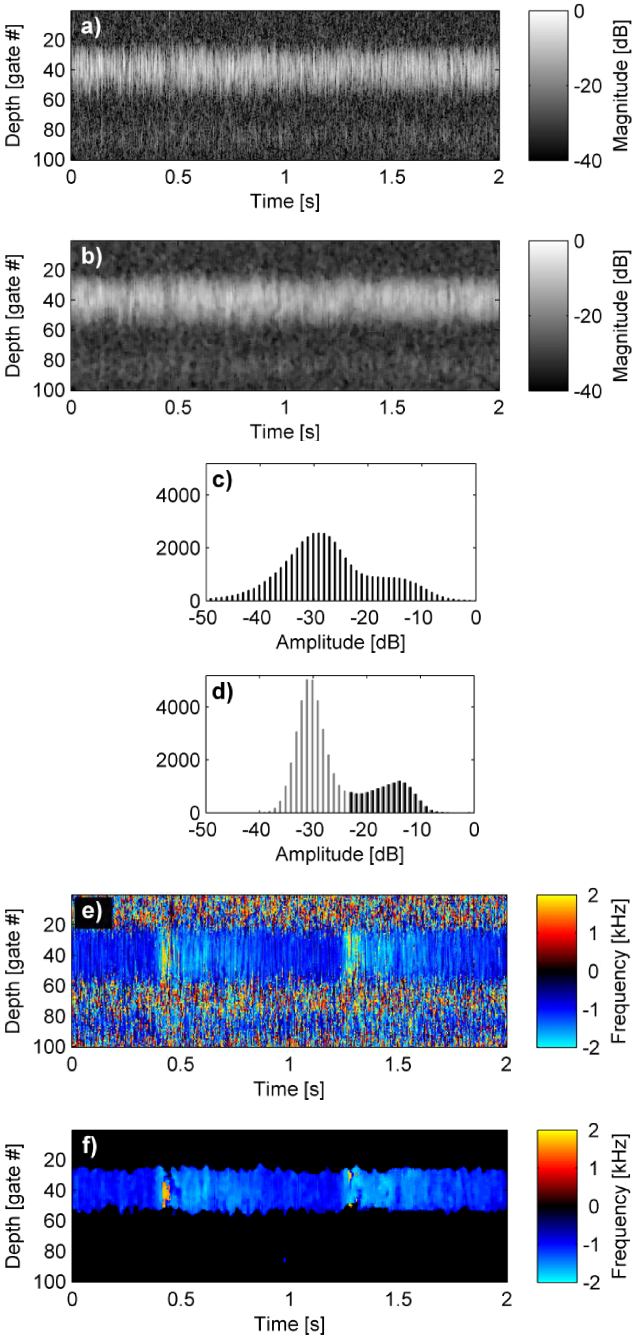

Fig. 9. Colour channel data at several stages of the background rejection algorithm: a) the raw AC map, b) the AC map after median filtration, c) the histogram of the raw AC map, d) the histogram of the filtered AC map, e) the raw map of Doppler frequencies, f) the map of Doppler frequencies after the background rejection.

In cases of low value of SNR, the above-mentioned distributions overlap so strongly that it is impossible to separate their maxima. Therefore, a median filtration is applied to the AC map (Fig. 9b), which narrows the histogram distributions (Fig. 9d). This usually allows to estimate the AC threshold level. However, if the algorithm is still unable to distinct the two maxima,

it searches for a local maximum of histogram's first derivative that is nearest to histogram's peak. Then the threshold value is chosen with the use of an arbitrary proportion parameter from between the derivative and histogram maxima.

As the AC threshold value is derived, all the Doppler frequencies which correspond to the AC values lower than the threshold level are set to zero, as they represent the stationary tissue.

The map of Doppler frequencies after the background rejection is ready to be displayed in a colour scale. However, to smooth the final image (Fig. 9f) a median filtration is applied. This solution performs better than the standard low-pass filter, as the smoothing does not go together with a blur effect.

3.3. Spectrum channel

The Spectrum mode enables an audio-visual presentation of Doppler data from a selected depth (gate). Actually, the audio output allows only a qualitative analysis and it does not provide additional information to those introduced by visual display. Nevertheless, it is still a useful tool which improves perception of the data (Ali *et al.*, 2008).

The Audio part of the Spectrum channel could pass the Doppler data straight to a sound card as the signal is in the acoustic band already. However, a distinction of directions of the blood-flows requires additional operations. The so called direction separation can be performed in several ways (Aydin *et al.*, 1994). The digiTDS employs a separation in frequency domain. This method starts with a Fast Fourier Transform (FFT) of the complex I/Q signal. The produced series of spectra are split into two channels containing positive and negative frequencies which represent flows directed towards and away from a probe respectively. The separated spectra are next back-transformed (inverse FFT) to the time domain, assembled into two continuous audio-tracks, passed to the sound card, and played in stereo mode.

The Spectrogram part of the Spectrum channel also starts with the FFT producing a series of spectra which are formed into the spectrogram (Fig. 10a). However, the result is noisy and difficult for automated analysis. Thus, the background rejection algorithm is applied. The algorithm is similar to the one introduced in Subsec. 3.2. Nonetheless, unlike in case of the color chain (where the main object – colour map – was modified based on the other object – AC map) it analyses only the spectrogram. The resulting image (Fig. 10d) is smooth (due to a median filtering involved in the algorithm) and devoid of background, hence it is more readable and better for further analysis. The final step is to derive an envelope of the spectrogram, which corresponds to maximal flow velocity as a function of time.

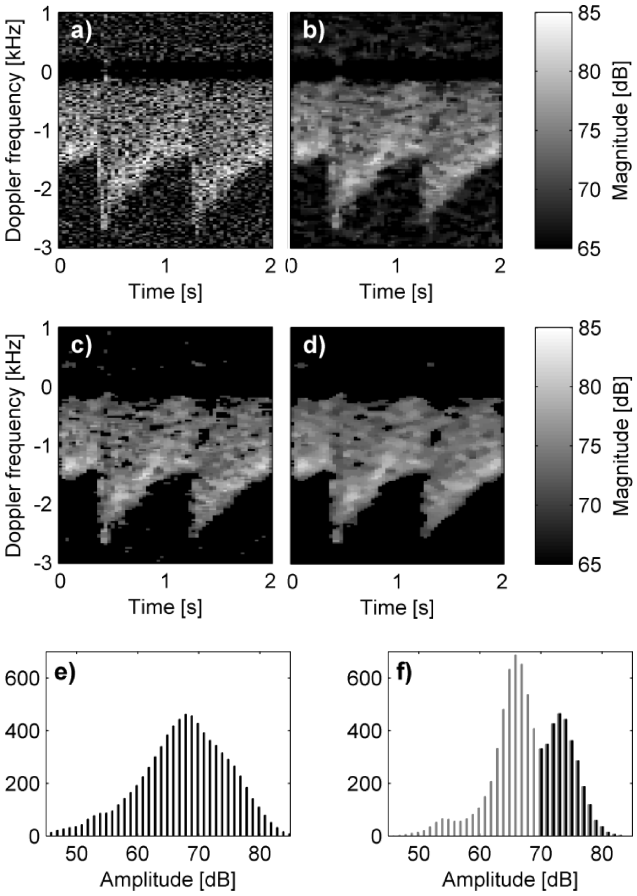

Fig. 10. Spectrum channel data at several stages of the background rejection algorithm: a) the raw spectrogram, b) the spectrogram after median filtration, c) the spectrogram after thresholding, d) the thresholded spectrogram after final median filtration, e) the histogram of the raw spectrogram, f) the histogram of the filtered spectrogram.

Furthermore, our system provides multi-gate processing which allows to observe and analyse the spectrograms at many different gates simultaneously. This feature also allows to reconstruct the flow velocity profile in real time and opens the way for an implementation of ultrasonic velocimetry (application which is already under way).

3.4. Software implementation

Digital signal processing software algorithms have been implemented using Intel® IPP libraries (Taylor, 2004) which use SSE (Streaming SIMD Extensions) vector extensions of ×86 family processors. The SSE extensions enable simultaneous execution of floating point operations on multiple data, which ensures a very high efficiency of multimedia applications (Lyons, 2004).

The control and user software (Fig. 11) is implemented in Microsoft® dotNET 3.5 framework and runs on Microsoft® Windows Embedded Standard 2009 platform. For communication with the digital mod-

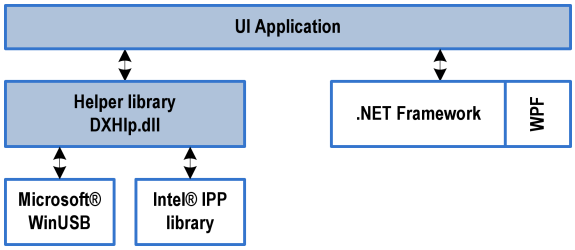

Fig. 11. PC software stack of the digiTDS system.

ule via USB interface, the Microsoft® WinUSB drivers were applied. User interface (Fig. 12) was created based on .NET Windows Presentation Foundation. In order to keep Doppler signal transmission as short as possible, the processing and the visualisation required optimal data buffering, processing optimisation, as well as multithreaded implementation.

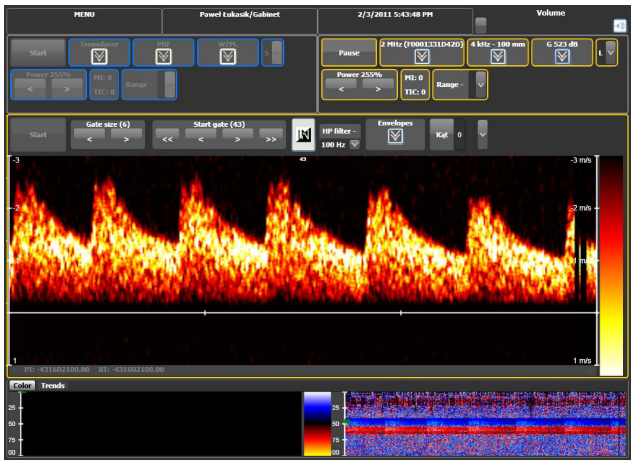

Fig. 12. User interface of the digiTDS. The Spectrum and Colour displays are in the middle and in the bottom of the image respectively.

3.5. Validation

The signal processing in digiTDS is based on conventional, frequently described Doppler algorithms. However, to prove that it meets the Doppler standards, its performance was verified through comparison with a SonixTouch Q+ device (BK Ultrasound, USA). Both systems were used to examine a flow in a Doppler phantom (Dansk Fantom Service, Model 453). The examination conditions (flow parameters, probe orientation, frequency, gate size, etc.) were identical or as similar as possible for both measurements. The maximum flow velocity measured with the digiTDS was −113 cm/s, while average sound velocity was −67 cm/s (negative values for flow away from the probe). These results are consistent with the spectrogram displayed by SonixTouch Q+ (Fig. 13). This confirms that the signal analysis performed in the digiTDS is correct.

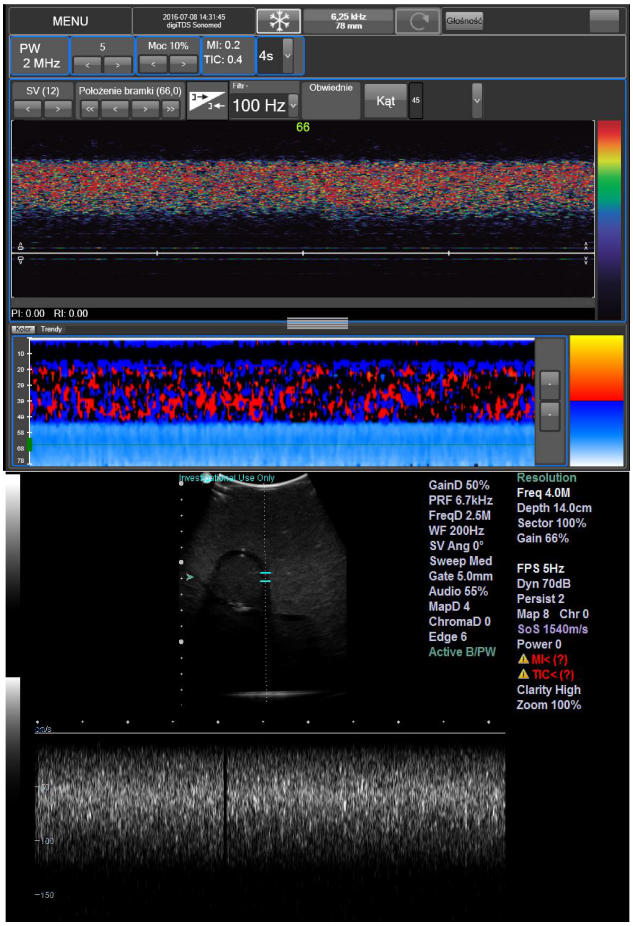

Fig. 13. Comparison of the displayed results in case of the digiTDS (top) and the SonixTouch Q+ (bottom).

4. Conclusions

4.1. Applications

Since the first application in 1982 Transcranial Doppler is accepted as a non-invasive way of viewing the blood flow in the cerebral (brain) arteries and veins. As a diagnostic tool it can be used at bedside to assess the cerebral vasculature in inexpensive, safe and reliable way (when compared with other techniques). It can be repeated multiple times or used for continuous monitoring if needed. Immediate, real time detection of changes in cerebrovascular hemodynamics is possible. It can be utilised by any medical specialty to evaluate several neurovascular disorders. The common Transcranial applications include: screening for intracranial diseases – MCA stem stenosis and occlusion, carotid siphon stenosis, distal vertebral stenosis, basilar stenosis, collateral flow, vasospasms. Transcranial is a clinical tool to help in the diagnosis of medical conditions such as cerebral emboli, stroke diagnosis and treatment, as well as vasospasm related to a subarachnoid hemorrhage.

The intracranial arteries may be examined through conventional temporal, foraminal, and orbital win-

dows. It is a "blind procedure": its accuracy relies on the knowledge and experience of a trained operator and interpreter. According to the literature, in 5% to 10% of cases, the sufficient penetration of the bone window cannot be achieved for ample insonation attributable to skull characteristics. Doppler is useful only if a reliable signal is found.

The digiTDS performance was tested on cases with the identified "poor acoustic window". The ability of the system to obtain simultaneous signals from different vessels with the reduced acoustic power emission was considered and tested.

4.2. Discussion

The paper presents the technical development of a new multigate Doppler device pertaining to the architecture of digital signal processing and task distribution between software and hardware in ultrasound diagnostic devices. The solutions reported in literature were reviewed and the similarities between the presented solutions and the SDR systems used in digital telecommunication were discussed. The two presented examples of combined hardware-software processing architecture in the ultrasound devices represent current state of the art. The experiences gained during designing and implementation of the digital processing algorithms on this platform show their unquestionable advantages, namely:

- possibility of algorithm migration between hardware and software solutions,
- possibility of equalisation of load distribution in all system elements and data transfer between sub-systems,
- possibility of optimisation of the selected system parameter (time delay, data transfer, power consumption, etc.) by changing the method/place of processing execution.

It is also worth noting that the problems can be encountered during system development requiring advanced real time processing, namely:

- difficulty in defining the required efficiency and throughput of each system component at the design stage,
- problems with operating the system in real time with minimal time delay of result presentation (image, audio),
- time synchronisation of hardware and software subsystems (particularly those controlled by not real-time operating system),
- verification and validation of the whole system, as required for medical device.

The future development of ultrasound medical systems will be interrelated with the development of electronics and digital signal processing systems. The present trend of extending the scope of software processing will be probably continued with the next generation of multicore GPP, DSP, and GPU. Rapid development of portable devices can be expected, due to the availability of increasingly fast, integrated and low-power System on Chip integrated circuits.

The developed Doppler system is a unique combination of the research equipment and the certified medical device. Its mixed architecture allows the implementation of the advanced signal processing while keeping the costs low. Further work will aim to implement methods for detection of microemboli at cardiological applications, and monitoring in assisting with the artificial heart ventricle.

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