

APPLICATION OF PULSE MODULATION TECHNIQUES FOR CLASS-D AUDIO POWER AMPLIFIERS

Zbigniew KULKA

Warsaw University of Technology
Institute of Radioelectronics
Electroacoustics Division
Nowowiejska 15/19, 00-665 Warszawa, Poland
e-mail: Z.Kulka@ire.pw.edu.pl

(received May 8, 2007; accepted June 26, 2007)

The class-D power amplifiers which operate in a switched mode have become an attractive alternative of the conventional analog power amplifiers class-A, B and AB in the field of audio applications. They offer high power efficiency compared to analog power amplifiers and can be realised as completely digital power amplifiers. This paper briefly overviews the basic concepts of analog and digital power amplification using the pulse-width and sigma-delta modulation techniques as well as novel approach based on a click modulation technique and class-D power stages.

Keywords: class-D power amplifier, pulse-width modulation, sigma-delta modulation, click modulation.

1. Introduction

Conventional analog power amplifiers utilizing transistors (bipolar, unipolar) or vacuum tubes as the output devices are used in the audio equipment since many years [1, 2]. Such amplifiers belong to the different classes depending on how much current is allowed to flow through the transistors or tubes in the power stage when they are not delivering power to the loudspeakers. Most conventional power stages are a variation of a configuration known as push-pull. In its elementary form, it uses two transistors or tubes: one for pushing current, or sourcing it, toward the loudspeakers, the other for pulling it back or sinking it. There are three basic analog audio power amplifiers, i.e. class-A, B and AB, which are also termed linear power amplifiers. The primary difference between linear and non-linear (switched mode) class-D amplifiers is the power efficiency [3, 4].

In class-A amplifier, for a sine wave input signal the output devices are continuously conducting for the entire cycle of the input signal, i.e. there is always bias current

flowing in the output devices. This configuration introduces the least distortion and is the most linear, but at the same time is the least efficient (up to about 50%). Class-B amplifier operates in the opposite way to class-A amplifier. The output devices conduct only for half the sine wave cycle, so that all of the output current comes either from the current-sourcing device or from the current-sinking one but never from both at the same time. This mode of operation is obviously more efficient than class-A (up to about 80%). The main problem with class B is with distortion at the crossover point, due to the time it takes to turn one device off and turn the other device on. Class-AB amplifier is a combination of the above two types and is the most popular audio amplifier. Both output devices are allowed to conduct at the same time, but just small amount near the crossover point. Hence each device is conducting for more than half a cycle but less than the whole cycle. Therefore, class-AB assure a reasonable compromise between linearity and power consumption at the efficiency up to about 70%. For real music signals and a common listening levels of about 30–40% of full volume, the efficiencies listed above are far lower. Therefore, it is necessary to dissipate a significant amount of heat from the linear amplifiers.

Class-D amplifier operates in a switched mode, i.e. its output devices act as switches and usually switch between two states, fully on and fully off, and than back again. In almost every practical class-D amplifier, power MOSFETs (metal-oxide semiconductor field-effect transistors) are used. Though real output devices with their static and switching losses will slightly reduce the efficiency, this discontinuous (nonlinear) mode of operation class D amplifier results in an outstanding high power efficiencies of 90–95%. This high power efficiency translates into lower power supply consumption and reduced heatsink requirements drastically. This is also the *first and basic reason* of interest in further development of an old idea of class-D amplification. Of course, class-D amplifier can reproduce only binary (two-valued) waves (hence named “digital amplifier” by analogy to the operation of digital logic circuits). To use it to amplify analog music signals, those signals have to be converted into a suitable square wave, containing a series of pulses switching class-D power stage. This signal conversion can be realized by different types of the pulse modulators [5].

Conventionally, reproduction of the sound from the digital signal sources, such as CD, DVD-Audio, Super Audio CD or DVD-Video players, requires intermediate digital-to-analog conversion followed by inefficient analog linear amplification (class A, B, or AB). On the contrary, the digital input class-D power amplifier makes it possible to build a full digital audio reproduction system, which performs the direct conversion of digital audio data into analog power without the intermediate digital-to-analog conversion stage. It is a very attractive idea and thus giving the *second important reason* for the use of the class-D amplification concept. Such a digital power amplifier is sometimes referred to as a power digital-to-analog converter.

Recently, the digital class-D audio power amplifiers are commonly found in two- or multichannel sound reproduction systems, e.g. in the home theater DVD-Video surround sound systems which require 5 to 7 power amplifier channels in one box with

acceptable size, in the active loudspeakers and in high-level power sound systems used in clubs and concert venues. More recently, digital class-D amplifiers have expanded beyond the multi-channel sound systems, showing up in battery-powered portable equipment like MP3 players with a miniature hard disc or flash card memories, portable CD and MD players, laptop and palmtop computers, cellphones, personal digital assistants, hearing-aid devices, car entertainment systems, etc.

2. Basic structure of class-D power amplifier

A simplified block diagram of a class-D audio power amplifier is shown in Fig. 1. It consists of a pulse modulator stage, a switched-mode power stage and a pulse demodulator stage. As it can be seen, when the modulation and demodulation processes are performed, both must correspond to each other, i.e. the demodulation process must be inverse to the modulation process.

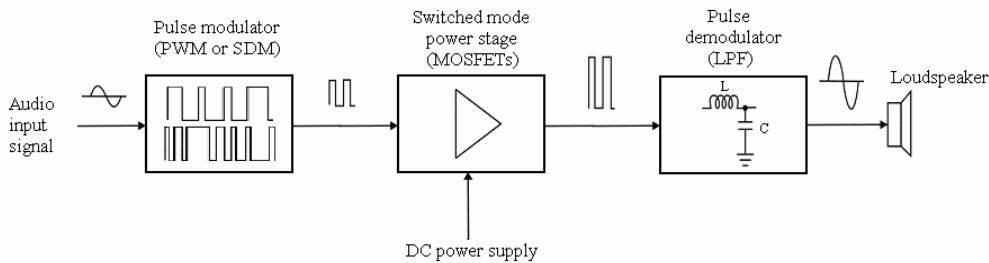


Fig. 1. Basic structure of the digital power amplifier.

A pulse modulator converts a low power audio signal, which may be analog or digital PCM (pulse-code modulation), into binary intermediate signal with a fixed level. This signal is fed to the switched-mode power stage, and then the amplified binary signal is demodulated by a passive low-pass filter (LPF) that reconstructs the audio signal by averaging the switching node voltage. The demodulation results in a power amplified analog audio signal which drives a loudspeaker.

2.1. Pulse modulator stage

There are two different methods of the pulse modulation. One of them is the well-established pulse-width modulation (PWM), which is used in many applications, for example, in the switch-mode power supplies (SMPS). PWM wave has a fixed pulse cycle time but its duty cycle vary according to the input signal amplitude. For small input amplitude the pulse width is small, while it is large for large amplitude. Such a signal conversion can be realized by the analog or digital pulse-width modulator (PWM). The second approach for the pulse modulation is to vary the pulse density depending on the input signal amplitude. In this pulse-density modulation (PDM), each sample at

the multiplies of the modulator clock rate can be seen as one single pulse. Converting large signal amplitudes results in a high number of samples being at the “high” state, while at small signal amplitudes most samples can be met at the “low” pulse level state. Therefore, this pulse conversion has no fixed cycle time, but can be considered to have a varying pulse frequency. PDM-based signal conversion can be realized by the analog or digital 1-bit sigma-delta modulator (SDM). So, the class-D amplifier concept leaves it as an option whether to choose an analog or a digital modulator design, resulting in an analog PWM or analog SDM class-D power amplifier respectively, as well as digital PWM or digital SDM class-D power amplifier respectively.

2.2. Class-D power stage

Class-D amplifier can operate in half-bridge or full-bridge configuration with two or four output devices, respectively, which are the power MOSFETs. The basic configurations of the class D power stage are sketched in Fig. 2.

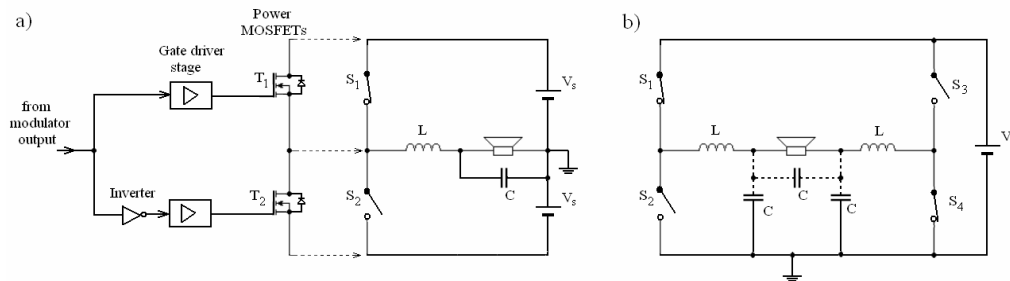


Fig. 2. Two basic class-D amplifier configurations: a) half-bridge, b) full-bridge, L,C – output filter elements.

In the half-bridge configuration (Fig. 2a), two power N-channel MOSFETs are used as switching devices S_1 and S_2 (also the P-channel and N-channel complementary pair can be applied). The symmetrical DC voltages V_S are needed for the operation. When S_1 is turned on and S_2 is off, the positive voltage V_S is applied to the load (i.e. to the filter and loudspeaker), and when S_1 is off and S_2 is turned on, the negative voltage V_S is connected to the load. Obviously, only one of the switches can be on at any time. To avoid a risk of short-circuit between the supply rails when both switches are on at the same time (a huge current can destroy MOSFETs), some dead-time, i.e. a small period where both MOSFETs are off, has to be introduced. For the lowest distortion, the dead-time must be as small as possible. Also timing will affect the efficiency and audio quality. To ensure fast rise/fall times of the MOSFETs, each gate driver must provide quite a high current to charge and discharge the gate capacitance during the switching interval. In half-bridge configuration, the power supply might suffer from energy being pumped back from the amplifier, resulting in supply voltage fluctuations when the amplifier outputs low frequency audio signals to the load.

In the full-bridge configuration (Fig. 2b), named also as H-bridge, only one DC supply voltage V_S is required but four switches are needed. With S_1, S_4 closed and S_2, S_3 open, the load is connected to the supply voltage V_S . In reverse situation, i.e S_1, S_4 open and S_2, S_3 closed, the load is also connected to V_S , what means that V_S appears twice across the load. The filter may be implemented by means of a single capacitor across the loudspeaker, by a pair of capacitors to ground, or in some cases by both (as shown by the dotted lines connecting the capacitors). Complementary switching legs in the full-bridge configuration tend to consume energy from the other side of the leg, so there is no energy being pumped back towards the power supply.

As it can be seen, the power stages from Fig. 2 are directly connected to the supply rails via low resistance of the switches. It is their weak point, because supply voltage variations caused mainly by the switching load currents and ripples introduce distortion, especially for single-ended connected speaker (as shown in Fig. 2a). The bridge-tied-load (BTL) speaker configuration (as shown in Fig. 2b) drives both speaker terminals from an H-bridge MOSFET stage. The differential structure of the bridge configuration has a benefit in audio performance because it can inherently cancel harmonic distortion components of even order and DC offsets (in half-bridge configuration the DC offset adjustment is needed). It is worth to notice that by changing the power stage supply voltages one can change the amount of amplification factor.

2.3. Pulse demodulator stage

The pulse demodulator stage in a form of low-pass filter (LPF) between the switching power stage and the speaker is required to remove the high frequency switching components and to reconstruct original shape of the audio input signal. As previously stated, a passive analog filter built with loss-free L-C elements is used. The LPF (usually of the second or higher order) is connected in series with the speaker impedance, thus it decreases the amplifier control over the speaker, especially at high frequencies. Therefore, the frequency transfer of the amplifier becomes load-dependent. In some cases the crossover filter of the speaker can be detuned because of interaction with the amplifier's low-pass output filter. To reduce the negative effects of the output filter, its cut-off frequency is typically chosen at about 60 kHz. Also the filter components suffer from non-linearities. In general, the filter has to be properly designed, ensuring the highest possible linearity up to the maximum power and over the full audio frequency range.

2.4. Class-D power amplifier imperfections

The major problem of the basic concept of the class-D power amplifier lies in the mismatching of modulation and demodulation processes. The reason of that are distortion and noise which are derived from errors arising in each stage of the amplifier. The nonlinear distortion produces new spectral components, which do not exist in the original signal. One common measure to quantify nonlinear distortion is the total har-

monic distortion (THD). However, class-D power amplifiers have different distortion mechanisms compared to analog amplifiers due to their switching operation. The spectrum of the power stage output pulses includes the desired audio input, but also several undesirable components which come from:

- distortion and noise, resulting from non-linearities in the modulation technique or modulator implementation;
- distortion and noise, resulting from nonlinear errors in the timing and shape of the output pulses, introduced by the power stage. For example, due to the necessary dead-time, effective pulse-waveform becomes load- and signal-dependent. Also, the output impedance of the DC supply voltages results in load- and signal-dependent pulse-heights;
- load-dependent frequency transfer (and the corresponding signal delay) of the amplifier due to interaction between the passive output filter and the complex impedance of the loudspeaker;
- the electromagnetic interference (EMI) emitted by the power devices due to their fast switching.

To eliminate or reduce the distortion-causing errors, different solutions have been proposed through the years. These include: application of the feedback techniques, introduction of the nonlinear distortion compensation methods with application of the digital signal processing algorithms, etc., which unfortunately lead to complexity of the class-D analog and digital power amplifier designs, increased by the need to conform to stringent EMC (electromagnetic compatibility) standards.

3. Analog and digital PWM

There are two main types of PWM which result in sampling of the audio signal: naturally sampled PWM (NPWM) and uniformly sampled PWM (UPWM). NPWM is naturally created in the analog PWM modulator, where low power analog audio signal is compared to a carrier (reference) signal. The carrier signal can be a sawtooth or triangle signal, corresponding to single-sided modulation (leading or trailing edge) and double-sided modulation, respectively. In other words, natural sampling is the instantaneous intersection of carrier and signal, and it is used to determine the switching instants of the pulse-modulated pulses. UPWM is typically generated digitally by directly translating an input sample to a pulse width.

Further modulation schemes are defined by the switching method which can be a two-level PWM or three-level PWM. Two-level PWM contains two possible output levels, high and low. Three-level PWM contains three possible output levels since a zero level is included. Class-D amplifiers typically use two-level rather than three-level PWM to control the switching power stage. Three-level PWM is more beneficial because it increases the efficiency of the full-bridge configuration, but at the same time, its control is more complex.

3.1. Analog PWM

An analog input class-D power amplifier uses an analog PWM modulator to drive a switching power stage. The PWM signal is generated by a voltage comparator (Fig. 3). An incoming audio signal is applied to one input of a comparator, and a carrier (modulating) signal, whose frequency is some multiple (e.g. 10–20 times) of the highest possible input signal frequency of interest (i.e. 20 kHz), is applied to the other comparator input. Figure 4 shows an example of NPWM waveform resulting from comparison of an analog input signal with a sawtooth carrier signal.

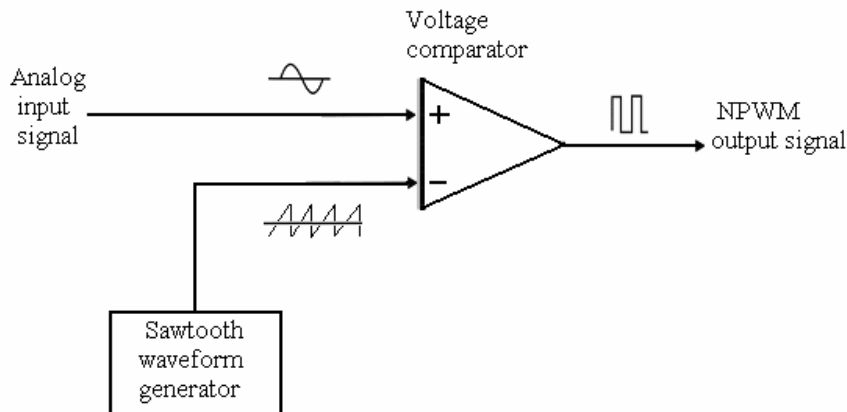


Fig. 3. Functional model of a trailing-edge NPWM modulator.

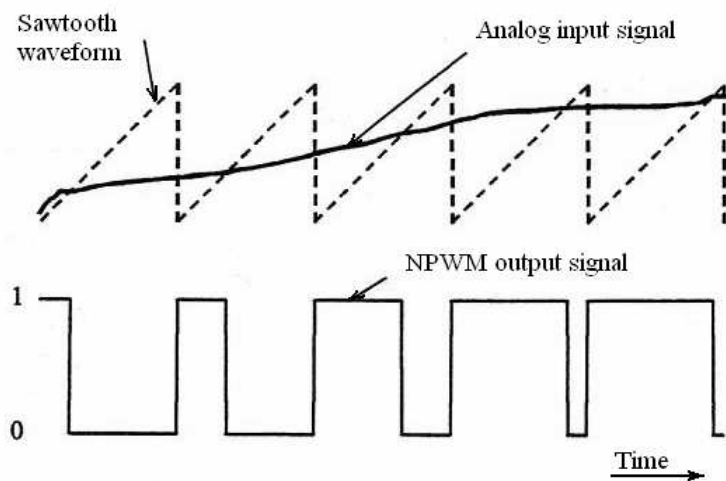


Fig. 4. One-sided, trailing-edge NPWM output waveform.

The spectra of various kinds of the PWM signals for single frequency sinusoidal input signals have been analytically determined using a two-dimensional Fourier series

[6–9]. Decomposition of the unity-amplitude single-sided (trailing edge) NPWM-output signal for modulation by a single tone input, $M \cos \omega_v t$, into sinusoidal parts, yields:

$$\begin{aligned} \text{NPWM}_{ss(t-e)}(t) = & k + \frac{M}{2} \cos \omega_v t + \sum_{m=1}^{\infty} \frac{\sin m\omega_c t}{m\pi} \\ & - \sum_{m=1}^{\infty} \frac{J_0(m\pi M)}{m\pi} \sin(m\omega_c t - 2m\pi k) \\ & - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{J_n(m\pi M)}{m\pi} \sin\left(m\omega_c t + n\omega_v t - 2m\pi k - \frac{n\pi}{2}\right), \quad (1) \end{aligned}$$

where variable ω_v is the angular input signal frequency, ω_c is the angular fundamental frequency of the PWM carrier, and k is the average amplitude of the unmodulated carrier. J_x denotes a Bessel function of the first kind.

The spectrum consists of the input frequency, the carrier and its multiples, and the sums and differences of the input signal and the carrier and its multiples. It is important that there are no harmonics of the input signal. However, the modulation products of the input signal and carrier fall back towards the input signal frequency, even though their amplitudes decrease. Thus, the carrier frequency should be much higher than the highest input frequency in order to have negligible modulation products affecting the audio baseband. In practical PWM designs that cover the whole audio band of 20 Hz to 20 kHz, the PWM carrier often is in the range of 200 to 500 kHz.

In analog PWM class-D amplifiers, the THD produced by inherent non-linearities and power stage non-idealities can be suppressed by using an analog negative feedback from the power stage output to the PWM modulator input [10], as shown in Fig. 5.

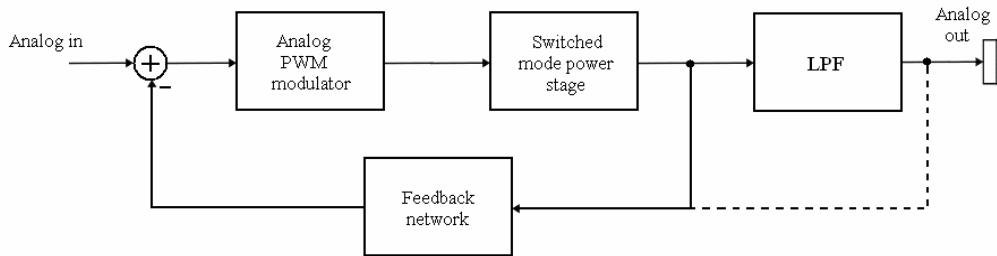


Fig. 5. Block diagram of PWM class-D amplifier with power stage-output feedback.

The negative feedback control loop reduces also the pulse-height errors resulting from the modulated DC power supply and output impedance. It would be better to take filter-output feedback (i.e directly from the speaker, marked in Fig. 5 by dashed line). However, due to the phase shift (delay) of the L-C filter, such an amplifier is prone to stability problems which in practice limits the gain of the feedback loop.

3.2. Digital PWM

The audio reproduction chain can be all digital if the analog PWM modulator is replaced by a digital PWM modulator, which is often referred to as PCM-PWM converter or an open-loop digital class-D amplifier. A digital PWM modulator converts amplitude samples into pulses with proportional width. The direct mapping of PCM samples into pulse-widths is commonly called UPWM, as mentioned earlier. There are four UPWM versions: leading or trailing edge single-sided UPWM and two forms of double-sided UPWM having either one or two input pulses per pulse (i.e. each edge is modulated independently by a different sample). In this paper only double-sided UPWM with one sample per pulse will be considered, as an example.

A functional model of a double-sided UPWM modulator is shown in Fig. 6, where the incoming signal first passes through a sample-and-hold circuit and then is applied to one input of a voltage comparator, and triangle waveform (carrier) at much higher frequency than the input signal is applied to the other comparator input. Figure 7 shows the double-sided UPWM waveforms.

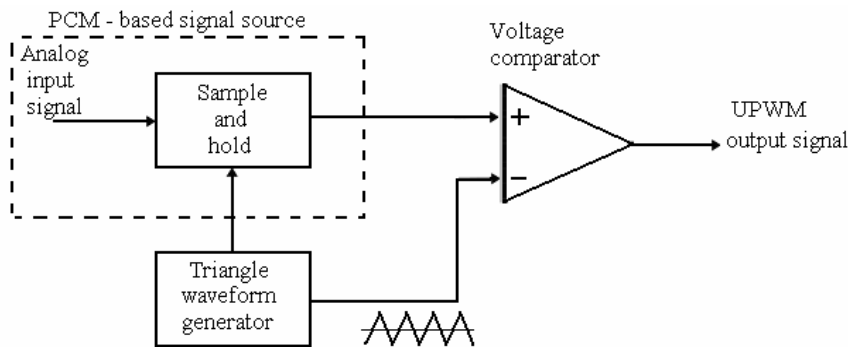


Fig. 6. Functional model of a double-sided UPWM.

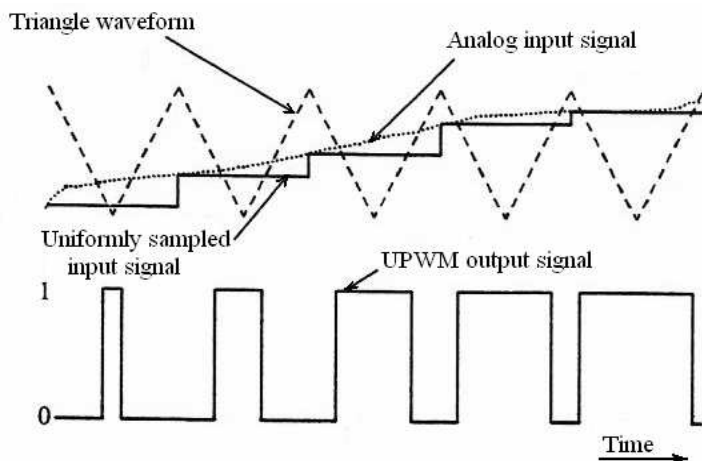


Fig. 7. Double-sided UPWM waveforms.

The double-sided UPWM-output signal for a single tone input, $M\cos \omega_v t$, can be decomposed as follows [6–9]:

$$\begin{aligned}
 \text{UPWM}_{ds}(t) = & k \\
 & + \sum_{n=1}^{\infty} \frac{2J_n\left(\frac{M\pi n\omega_v}{2\omega_c}\right)}{\pi n \frac{\omega_v}{\omega_c}} \sin\left(n\left(1 - \frac{\omega_v}{\omega_c}\right)\frac{\pi}{2}\right) \cos\left(n\omega_v t - \pi n \frac{\omega_v}{\omega_c}\right) \\
 & + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2J_n\left(\frac{M\pi n\omega_v}{2\omega_c}\right)}{\pi\left(m + n \frac{\omega_v}{\omega_c}\right)} \sin\left(\left(m + n\left(1 - \frac{\omega_v}{\omega_c}\right)\right)\frac{\pi}{2}\right) \\
 & \cdot \cos\left(n\omega_v t + m\omega_c t - \pi n \frac{\omega_v}{\omega_c}\right). \quad (2)
 \end{aligned}$$

The UPWM signal spectrum is characterized by a harmonic content in the audio baseband, and also modulation products of the carrier and input signal are presented. As can be seen in Fig. 8, the UPWM process introduces harmonic and non-harmonic distortion [11]. While UPWM is relatively simple to obtain, it does generate harmonic distortion, which NPWM does not.

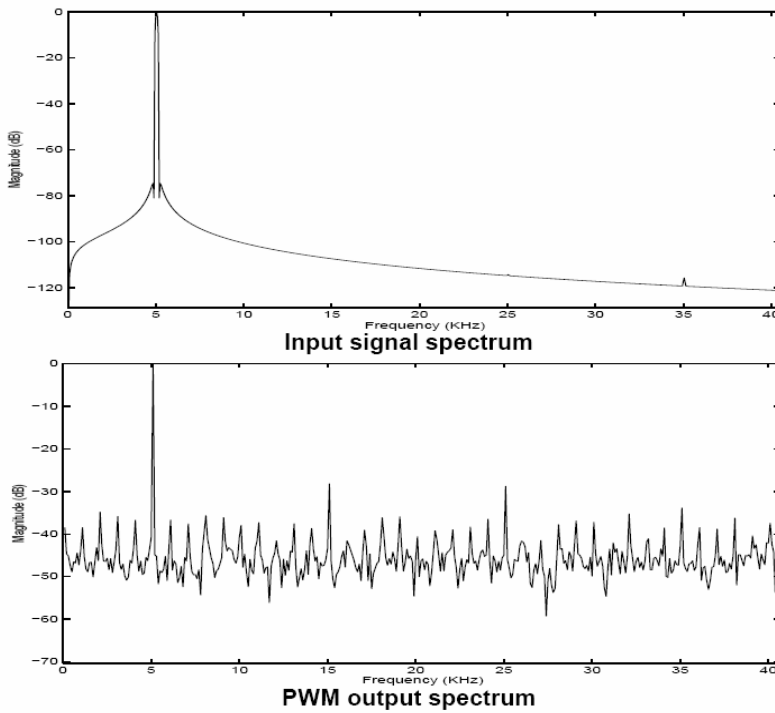


Fig. 8. Simulated spectra from the UPWM process [11].

The direct conversion of a digital PCM signal, determined by the word resolution expressed as the number of bits (N) and sampling frequency (f_s), to a UPWM signal, is conceptually simple but the hardware realization is difficult. The problem arises because an amplitude resolution of PCM signal has to be transformed into a time resolution of PWM signal what results in a need of having 2^N time resolutions per PCM sample. Figure 9 shows a digital PCM-UPWM (double-sided) counter type modulator that converts a PCM signal (N bits/ f_s) to a UPWM signal at the carrier rate f_c equal to the sample rate f_s of the PCM signal.

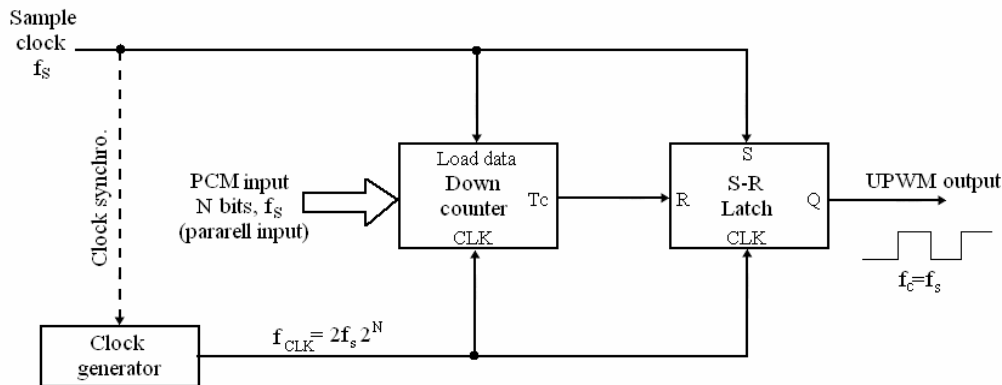


Fig. 9. Counter type digital PCM-UPWM converter.

To obtain the required time resolution of the UPWM output, the counter has to be clocked at twice the rate compared with the single-sided modulation, i.e. $f_{CLK} = 2 \cdot f_s \cdot 2^N$. Since audio systems operate with $N = 16$ – 24 bits and sampling frequencies $f_s = 44.1$ – 192 kHz, the necessary counter speed in this direct implementation is in the GHz range and it is a fundamental limitation in counter-type digital PWM modulators. For example, taking into account only the CD format, i.e. $N = 16$ bits and $f_s = 44.1$ kHz, the down counter clock would need to run at $f_{CLK} = 5.78$ GHz, what is clearly impractical.

The clock frequency may be reduced to several tens of MHz using digital signal processing in terms of oversampling and noise shaping, preceding the digital PCM-UPWM converter (Fig. 10).

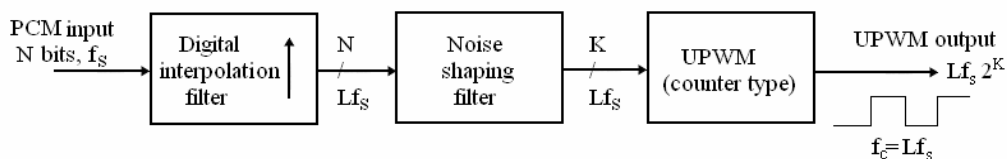


Fig. 10. Digital PCM-UPWM conversion using interpolation and noise shaping.

The PCM input signal (N -bit/ f_s) is first upsampled by a factor L using the digital interpolation filter and then requantized to K bits (where $K < N$) in the R -order noise

shaping filter; these shapes increased the requantization noise out of the audio baseband. This reduces the required clock rate for the counter (i.e. reduces time resolution). Usually, the digital interpolation filter is realized as a linear-phase FIR filter based on the polyphase decomposition of its transfer function. The use of oversampling and noise-shaping means that UPWM modulators share a lot of similarities with the sigma-delta modulators (SMDs) which will be described in more detail in one of the following sections. The requantization to $K = 6\text{--}9$ bits combined with oversampling ratio $L = 4\text{--}16$ makes a reasonable compromise that enables audio band quality to be maintained with an $R = 3\text{rd} - 5\text{th}$ order noise shaper [8].

Although application of the interpolation and noise-shaping greatly reduces the PWM timing clock requirements, it does not eliminate the distortion in the audio baseband which still exists. To improve the UPWM linearity, different methods are used.

3.2.1. Open loop PWM correction

In the last two decades a number of linearization methods have been developed, e.g. linearized PWM (LPWM), pseudo-natural PWM (PNPWM), weighted PWM (WPWM), dynamic filtering (DF) and so on [8, 9]. Most often the precompensation-based methods are used, where the PCM data are predistorted before they are fed into the PCM-PWM conversion process such that the PWM-nonlinearities are compensated [13–16]. A typical simplified block diagram of a PCM-PWM system including interpolation, correction, noise-shaping and UPWM is shown in Fig. 11.

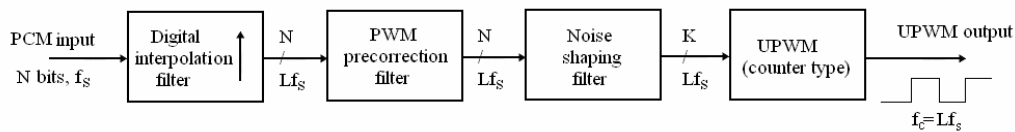


Fig. 11. Improved digital PCM-UPWM modulator using precompensation.

The correction algorithms should be made for easy implementation on custom designed circuits (e.g. using field programmable gate array – FPGA) or digital signal processors (DSP).

A bit different method of precompensation is based on application of the artificial neural networks [17]. First, a model of the digital amplifier using a neural network is constructed and next, using this model, the artificial neural network model of a predistortion filter is trained so that the combined system, including the digital amplifier and predistortion filter, produces a corrected output.

3.2.2. Closed loop PWM correction

In some applications the closed loop methods are proposed, where the nonlinearities are reduced by the feedback loops. A feedback loop around the modulator and power stage has not been used previously on pure digital class-D amplifiers because of difficulties which are mainly associated with the fact that the output of the amplifier is in

the analog domain while input, where the feedback has to be applied, is in the digital domain (this is why they have been named open-loop designs). In order to use feedback, an analog-to-digital converter (ADC) needs to be a part of the feedback loop. The performance of the ADC in terms of distortion and noise should be as good as the desired overall performance of the amplifier, and in addition, the delay (latency) of the ADC needs to be low for the feedback to be effective. Standard sigma-delta converters which operate with high oversampling ratios are not well suited for feedback applications due to the latency of the long linear phase FIR filters used for decimation. Therefore, a conventional multi-bit ADC or a low-bit sigma-delta ADC are rather preferred than the one-bit sigma-delta ADC [18]. Additional difficulties arise from the non-linearity of UPWM mainly used in digital class-D amplifiers as well as from variations in the power supply. The block diagram of the digital class-D amplifier with ADC-based negative feedback loop is shown in Fig. 12.

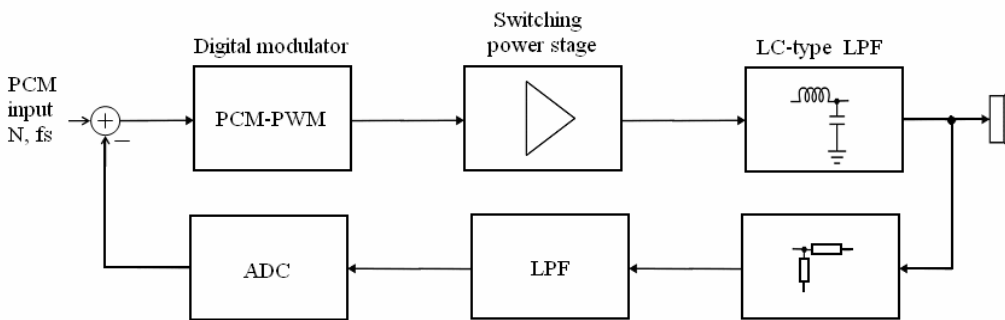


Fig. 12. Digital class-D amplifier with feedback.

The attenuator and low-pass filter are used in front of the ADC to attenuate the feedback signal and filter out the components around the ADC sample rate that might alias back into the audio baseband, and to attenuate the signal at the PWM switching frequency and its harmonics.

All the mentioned above difficulties have been overcome in a sophisticated design, so-called second generation intelligent digital PWM class-D audio amplifier controller IC with the ADC-based feedback [18]. This all-digital design includes feedback signal and power supply feed-forward technique are used to correct for power supply variations, non-linearity and other distortion-including mechanisms. In the next reference [19], the digital PWM class D amplifier for car use is presented. The developed amplifier utilizes a feedback system only on the power stage. The feedback system is composed of an analog correction circuit, and a feedback circuit which gives a constant attenuation. The correction circuit receives a PWM signal from PCM-UPWM converter and an attenuated PWM feedback signal from the switching output stage, then it compares these signals and outputs the error corrected PWM signal to the switching output stage.

Two other references are also interesting. The first one [20] describes a half-digital and half-analog audio power amplifier, where a simple digital four-output PWM system with power stages and output L-C filters creates four tracking power rails to a

fully differential class-AB power amplifier, preceded by a 16-bit audio digital-to-analog converter (DAC). The second one [21] describes an open-loop digital class-D amplifier which includes digital PWM modulator with power supply correction and a single-ended speaker load. The PWM modulator can be viewed as the digital equivalent of an analog class-D amplifier with feedback. Two 1-bit sigma-delta ADCs are used to supply the PWM modulator with the actual supply voltage levels to adapt its PWM output accordingly. The power supply correction is based on the observation that if the supply voltages become, for example, smaller, the amplitude of the incoming PCM audio stream to the digital PWM modulator must be made larger.

4. Analog and digital SDM

A next major development consists in the use of sigma-delta modulation (SDM) in class-D audio power amplifiers [22, 23]. The analog and digital sigma-delta modulators (SDMs) are now widely used in low-bit (multilevel) audio analog-to-digital and digital-to-analog converters, respectively. This form of modulation which includes oversampling, one-bit (two-level) coarse quantization or requantization (truncation) and spectral quantization (requantization) noise-shaping, is also suitable for analog and digital SDM audio power amplification. However, the output of the SDM can not be connected directly to the input of the class-D switching power stage (as shown in Fig. 1). On the one hand, to achieve the sufficient audio band signal-to-noise ratio (SNR), the typical oversampling ratios $L \geq 64$ is needed what results in the average pulse repetition frequency (PRF) above 1 MHz at the output of the SDM. On the other hand, to achieve high efficiency (i.e. low switching losses in the output stage) and proper linearity for acceptable audio quality, the average PRF at the SDM output has to be in a range of 300–500 kHz. So, the special algorithms and SDM structures have to be used to reduce the high PRF without severe impacts on the audio signal quality.

4.1. Analog SDM

The block diagram of a single-loop analog SDM is shown in Fig. 13a. It comprises a 1-bit ADC (quantizer), a 1-bit DAC, and a loop filter in a feedback loop.

The ADC introduces high-level quantization noise, which is spectrally shaped according to the loop filter to minimize the base band content of the noise at the expense of higher noise above the audio base band. The modulator operates on an oversampled input (Lf_S) to give an increased bandwidth in which the high-frequency noise is shaped. The modulator operation can be described as a discrete-time system in the z domain (Fig. 13b), in which the quantization noise is modelled as an additive white noise $E(z)$. For an input signal $X(z)$ and a loop filter $H(z)$, the modulator output is given by

$$Y(z) = \frac{H(z)}{1 + H(z)}X(z) + \frac{1}{1 + H(z)}E(z) \quad (3)$$

$$= STF(z)X(z) + NTF(z)E(z), \quad (4)$$

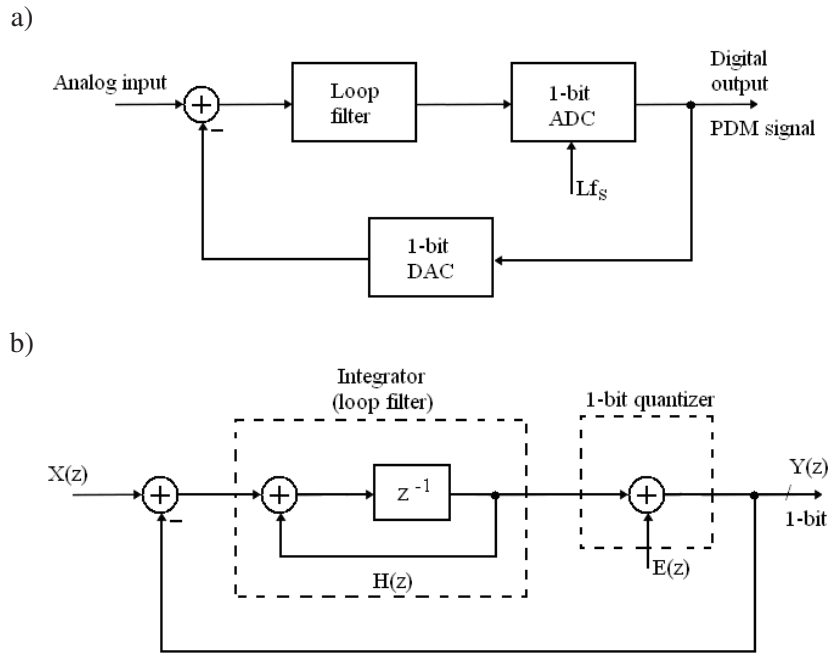


Fig. 13. Single-loop analog SDM: a) block diagram, b) first-order discrete-time model.

where

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z - 1}, \quad (5)$$

and $STF(z)$ and $NTF(z)$ are the signal and noise transfer functions respectively. The shaping of the quantization noise by the loop filter is described by the $NTF(z)$, which is usually designed as a recursive R -order high-pass filter with high attenuation in the baseband and minimum gain at higher frequencies to satisfy the stability requirements. In the simplest case, the low-pass filter (loop filter) is an integrator with a transfer function (5), resulting in the first order ($R = 1$) noise-shaping. In a single-loop configuration, the order of modulator is determined by the number of noise-shaping stages (integrators) within the loop. The continuous-time (CF) and/or discrete-time (DT) integrators can be used in a loop filter. The noise transfer function for the R -order noise-shaping is given by

$$NTF(z) = (1 - z^{-1})^R. \quad (6)$$

One can say that the higher is the order of the modulator, the greater will be the SNR in-band for a given oversampling factor L . As it is known, first and second order SDMs are inherently stable, and single-loop analog modulators of 3-rd order or higher are only conditionally stable. In practice, it is possible to prevent the SDM from becoming unstable by choosing appropriate gain coefficients and restricting the modulator's dynamic range. Higher order modulators also provide reduction of the idle pattern tones (typically in a form of limit cycles oscillations) and noise modulation. If needed, the suitable dither signal can be used (added before the quantizer).

There is a number of the loop filter configurations which can realize higher order noise transfer functions. Usually the noise-shaping structures called “cascade-of-resonators, feed-forward form” of orders up to 7-th are used. Figure 14a shows an example of a 1-bit analog SDM that consists of a 5-th-order Butterworth loop filter as a cascade of an integrator (I_1) and two resonators (consisting of integrators I_2 and I_3 with feedback by b_1 , and I_4 , I_5 with b_2).

Spectrum of the SDM output signal is shown in. Fig. 14b. The effect of the resonators reduces low-frequency noise by placing $NTF(z)$ zeroes (notches) at 10 kHz and

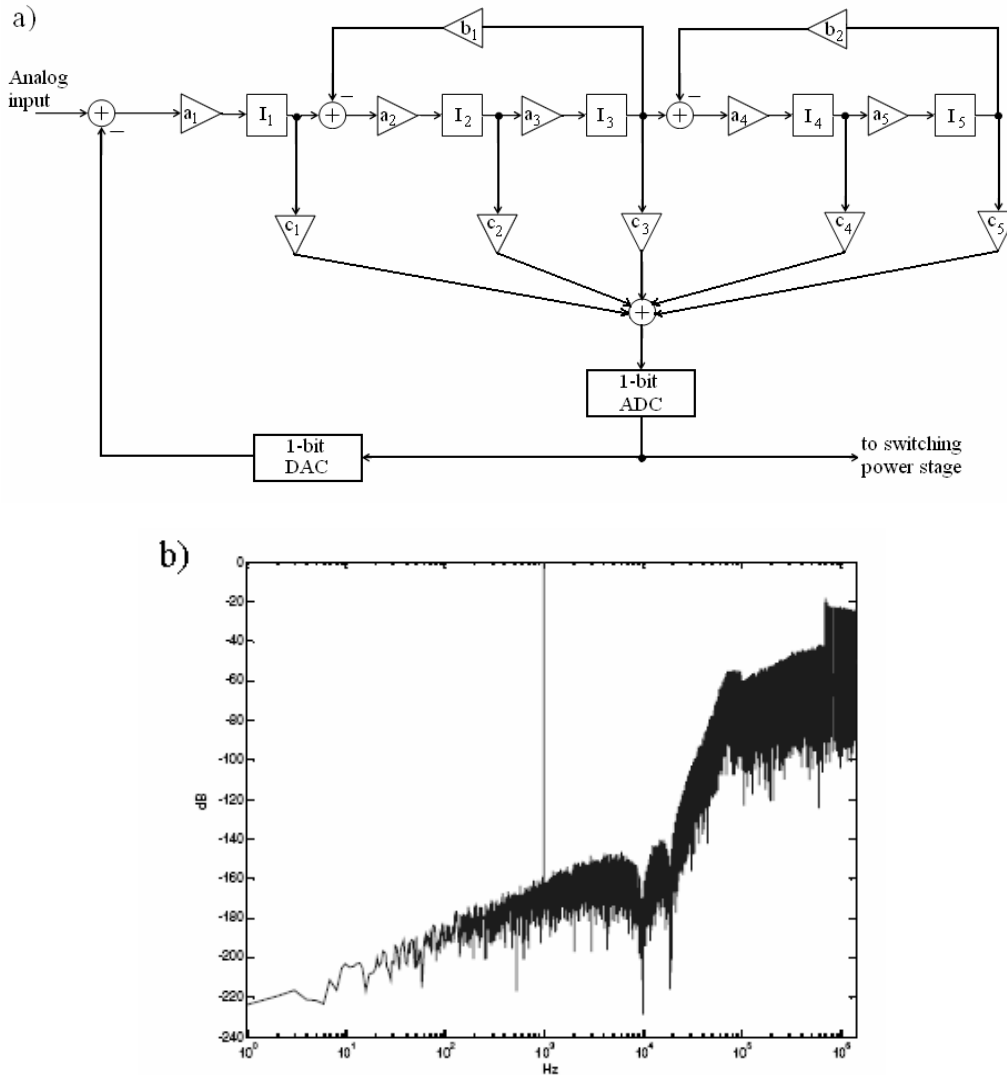


Fig. 14. 1-bit analog SDM: a) SDM structure, b) spectrum of 5th order SDM output signal with 1 kHz, 0 dB input signal; I = integrator.

19 kHz. The optimal set of coefficients $[a_i]$, $[b_i]$ and $[c_i]$ can be determined through simulations choosing coefficients values to be powers of two.

Analog SDM class-D amplifiers (as analog PWM class-D amplifiers) have significant advantage, that the switching power stage can be incorporated into the feedback loop.

The feedback loop (Fig. 15) reduces the influence of the power stage errors on the output signal quality and also reduces sensitivity to the clock jitter. For example, an integrated stereo class-D amplifier where 1-bit, feedforward 7-th-order SDM is used instead of the PWM modulator, is reported in [24]. To lower the output bit rate and switching losses, hysteresis is added to the quantizer with its dynamically adjusted amount. This yields average PRF between 450–700 kHz, depending on the input level.

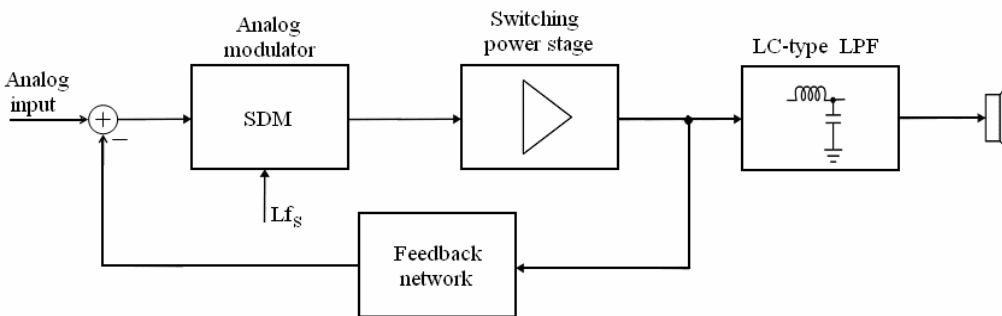


Fig. 15. Block diagram of an analog input SDM class-D power amplifier.

4.2. Digital SDM

The digital single-loop sigma-delta modulators (SDMs) can be classified by the order and the type of the feedback signal (MSB or LSB's error feedback). There are two basic configurations of the single-loop 1-bit digital SDMs (the DACs are not needed). The first one with MSM feedback is shown in Fig. 16a. It consists of the low-pass filter (loop filter) with transfer function $H(z)$ in which the integrators are replaced by accumulators, and the requantizer (truncator) which cuts off the MSB fed to the output and fed back to the input. The truncator is modelled as a summing node with additive white truncation noise.

The useful alternative of the first configuration is the second one, shown in Fig. 16b, called error feedback configuration, where the MSB is fed to the output and the LSB's are fed back to the input through the loop filter. Both configurations output digital words with a word length 1-bit and data rate Lf_s . Of course, to obtain the truncation noise-shaping effect, the input PCM signal before the modulator must be oversampled using the digital interpolation filter. Because both, i.e. analog and digital SDMs, share the same principle of the feedback loop filter action, the noise-shaping results and formulas describing noise transfer functions are the same. Since the noise-shaping loop in a digital SDM is a pure digital circuit, the stability of the loop can be assured even if the loop order is high.

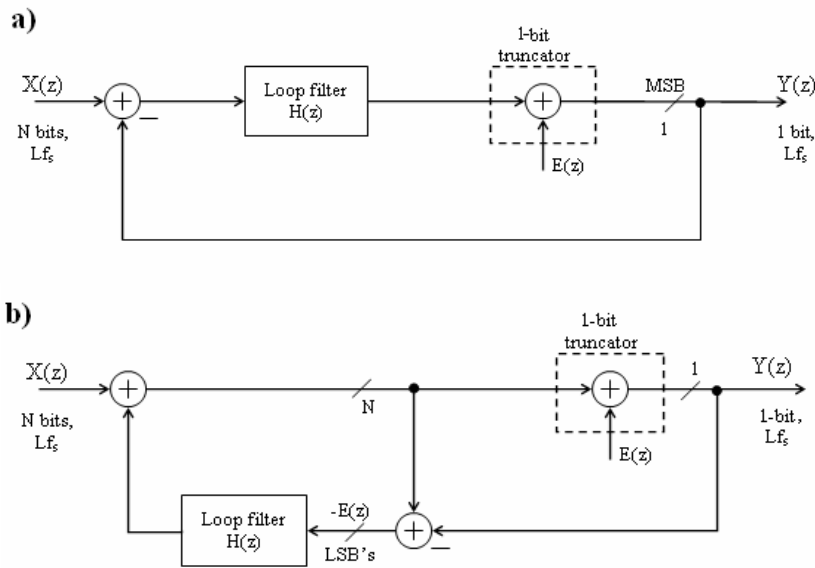


Fig. 16. Block diagrams of the single-loop digital SDM configurations: a) 1-bit modulator with MSB feedback, b) 1-bit modulator with LSB's error feedback.

The block diagram of a digital input SDM class-D power amplifier is shown in Fig. 17. For such a power amplifier, the SDM generates a 1-bit data stream with high resolution in the base band (> 16 bits for audio) but a low average PRF is necessary to reduce power dissipation in the power stage. Also in this case, the ADC-based feedback around the power stage can be used (see Fig. 12).

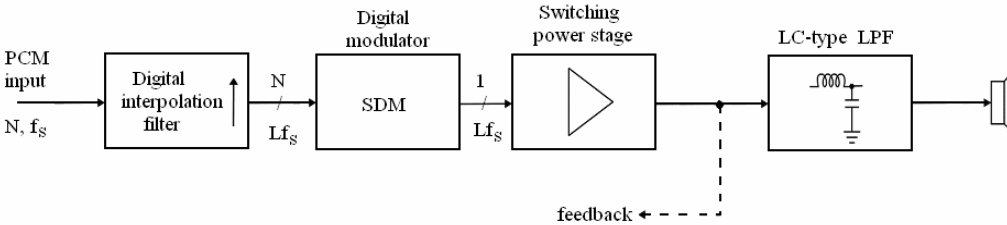


Fig. 17. Block diagram of a digital input SMD class-D power amplifier.

Several methods have been developed to reduce the average PRF, as for example, detection of high-frequency pulse patterns, inverting certain bit-states outside of the loop, pulse group modulation, bit-flipping, and a method based on characteristics of the *NTF* of the SDM loop [23]. The main goal, in general, is that the pulse signal has to be modified to become more uniform in terms of the local PRF, but the required SNR and stability performance should be maintained.

As an example, Fig. 18a illustrates the principle of the so-called “bit-flipping” algorithm [11, 23, 25], The idea is to selectively invert the state of the quantizer output

so that, e.g., the bit pattern of Fig. 18b is converted to the grouped pattern of Fig. 18c. Every bit inversion introduces an additional error equal in magnitude to the quantizer interval but occurring within the feedback loop, so that it is spectrally shaped together with the quantizer error. The inversion error also helps to decorrelate the quantizer error from its input. Bit-flipping occurs when the PRF exceeds a predetermined target (f_t). The control can be implemented as a counter which counts down every sample and counts up to M steps if the transition occurs between the current and previous output bits. A counter value greater than zero indicates that the target rate is exceeded and a bit-flipping should occur. For oversampling ratio L and sampling rate f_S , the value of M is given by $M = Lf_S/2f_t$. A target PRF of around $f_t = 350$ kHz is required to yield low switching losses in the power stage, leading to a value $M = 4$ for $L = 64$ and $f_S = 44.1$ kHz. The *NTF* defines the spectral shaping of the error introduced by the 1-bit quantizer (Q) and the bit-flipper (BF).

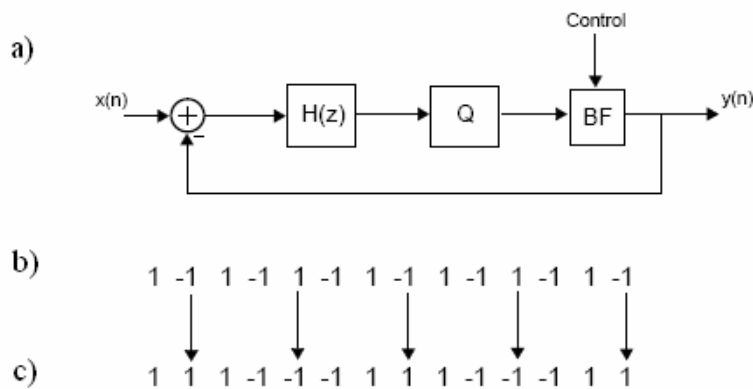


Fig. 18. Principle of the bit-flipping algorithm: a) block diagram of bit-flipping SDM, b,c) bit-flipping inversion.

An interesting concept is reported in [26]. The reference describes a digital PWM power audio amplifier which consists of a low-bit SDM followed by a digital PWM and a power stage. To remove the distortion, the correction factors are added to each accumulator of a 5-bit (32 levels) SDM loop. This results in a significant improvement in the distortion performance of the amplifier (a dynamic range of 100 dB is obtained with all harmonics suppressed below 102 dB).

5. Click modulation

The click modulation (CM) technique was invented by LOGAN [27]. The analytic derivation of this technique is too complex to be shown in this paper. CM allows the generation of a width-modulated pulse stream, whose spectrum has a separated base-band (free of any distortion), as opposed to the modulation techniques discussed in the

previous sections. This type of modulation is also named *Zero-Position Coding with Separated Baseband* (SB-ZePoC). In addition, a click modulated pulse stream does not require any oversampling, and satisfies the minimum requirements of the sampling theorem. CK-based PWM seems to be very well suited for digital power amplification, as it results in the theoretically minimal pulse rate thereby lowering the speed requirements of power switch elements and the digital modulator clock. However, the drawbacks of this technique are the heavy DSP computation rate, and very sharp demodulating passive L-C output filters.

In the modulation scheme, analytic signals that do not have a negative frequency content are used. Owing to this fact, a Hilbert transform will be incorporated. In the following, the resulting steps necessary to transform a given input signal $f(t)$ into a binary (square wave) signal $q(t)$ whose spectrum is the same as of $f(t)$ in the baseband, are summarized in Fig. 19.

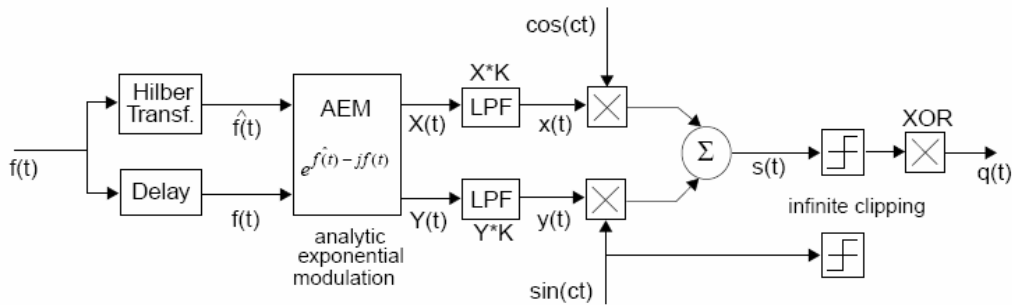


Fig. 19. Block diagram of binary click modulator (SB-ZePoC) system with separated baseband.

First, an input signal $f(t)$ is converted into an analytic signal $F(t)$ by adding its Hilbert transform as imaginary part, i.e.

$$F(t) = f(t) + i\hat{f}(t). \quad (7)$$

Next it is fed to an analytic exponential modulator (AEM) which evaluates the signal

$$Z(t) = X(t) + iY(t) = e^{-iF(t)}. \quad (8)$$

Then both the real and imaginary parts are low-pass filtered, resulting in the signal $z(t) = x(t) + iy(t)$. A single sideband (SSB) signal $s(t)$ is then created by multiplying real and imaginary parts of $z(t)$ appropriately by $\cos(ct)$ and $\sin(ct)$

$$s(t) = \text{Re} \{ z(t) e^{-ict} \} = x(t) \cos(ct) + y(t) \sin(ct). \quad (9)$$

Next clipping (signum) of $s(t)$ and $-\sin(ct)$ as well as multiplying the resulting signals is performed in order to form a binary signal $q(t)$ with separated baseband

$$q(t) = -\frac{\pi}{2} \{ \text{sgn } s(t) \} \cdot \{ \text{sgn } \sin(ct) \}. \quad (10)$$

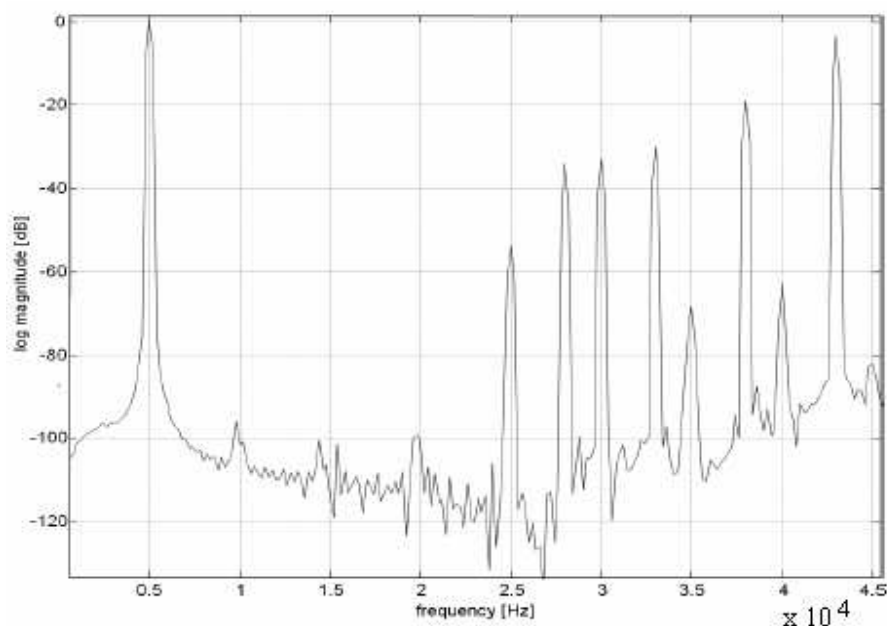


Fig. 20. Simulated magnitude spectrum of the $q(t)$ signal for full scale input tone at 5 kHz.

Simulated spectrum of the signal $q(t)$ is shown in Fig. 20 [28]. As can be seen, the noise floor is below 100 dB and the audio baseband is free of any distortion terms.

The application of CM to audio class-D power amplifiers was proposed a few years ago [29], and the practical implementation and measurement results of a first discrete real-time full audio band of the novel SB-ZePoC system was next reported in [30]. However, up to five digital signal processors (DSP) are needed to implement a real-time click-modulated audio power amplifier. On the contrary, the off-line CM coding concept is reported in [31]. The authors asserted, that many portable audio applications (CD or MP3 players, and so on) do not require real-time processing because they reproduce recorded music. Therefore, there is no need for a real-time implementation of the CM algorithm. The coding algorithm can be performed off-line using software routines to yield a stored file of time-switching instants. The algorithm needs to be performed only once for each piece of music, and the data file can be stored for later use in the audio player. The block diagram of the proposed digital amplifier with a click-modulated input is presented by the authors.

6. Conclusions

The basic concepts of high efficiency class-D power amplification based on different pulse modulation techniques were presented in this paper. The analog input and digital input class-D amplifiers utilizing now modern fast power MOSFETs which offer better-

controlled output switching, and the computational effective digital signal processing devices which make the possible to implement sophisticated modulation algorithms to optimize the performance of the amplifiers, were described. Such amplifiers are commercially available today and it seems that they will be dominant in the future, because of their high power efficiency, easy integration and cost-effective applications. Although the audio industry is moving or has already moved toward digital sound systems, the conventional linear power amplifiers still play and will play an important part in the sound reproduction systems. It is well known that high performance valve amplifier (in particular push-pull class-A) is the first choice for high-fidelity audio system because it gives the best listening results in a subjective sound quality assessment.

The battery-powered equipment is a prime target for the PWM and SDM class D amplifiers. Now, semiconductor companies like Texas Instruments, Cirrus Logic, National Semiconductor, Maxim, Tripath, Philips, STMicroelectronics and others, offer amplifier integrated circuits (ICs) with switching devices on-chip for mono and stereo applications at the low (typically a few watts) output power levels. Class D's efficiency lengthens the battery life and makes it possible to reduce or eliminate the heatsinks, without unacceptable sound quality sacrifices.

For the medium and high power output levels, i.e. from a several tens watts to as much as a few kilowatts, the semiconductor companies, like the mentioned above Philips and Tripath and others like Behringer, Microsemi's Linfinity division, and Zetex, all offer products named controller ICs. These devices can control the power MOSFET stages which are installed with the suitable heatsinks and low-pass output filters outside the controller chips. Controller ICs allow significant latitude in output power that is mainly a function of power stage supply voltage levels and power MOSFETs selection. They are used, for example, to build multi-channel class-D audio amplifiers for surround sound home theatre systems and active loudspeaker systems for home and professional audio as well as for live sound applications.

References

- [1] MORENO S. S., *Class D audio amplifiers – theory and design*, Elliot Sound Products, June 2005, www.sound.westhost.com/articles/pwm.htm
- [2] HONDA J., ADAMS J., *Class D audio amplifier basics*, International Rectifier, Application Note AN-1071.
- [3] ROSE D., *A comparison of modular state-of-the art switch mode and linear audio power amplifiers*, Proc. of the AES 112-th Convention, paper 5504, Munich, May 10–13, 2002.
- [4] BELL C., SIBSON I., *A comparison of digital power amplifiers with conventional linear technology: performance, function and application*, Proc. of the AES 119-th Convention, paper 6551, New York, October 7–10, 2005.
- [5] KOSTRZEWA M., KULKA Z., *Application of pulse modulators in digital audio amplifiers* [in Polish], Proc. of the 11-th International Symposium ISSET'2005, Cracow, June 23–25, 2005.

-
- [6] GOLDBERG J. M., SANDLER M. B., *Noise shaping and pulse-width modulation for an all-digital audio power amplifier*, J. Audio Eng. Soc., **39**, 6 (1991).
- [7] NIELSEN K., *High-fidelity PWM-based amplifier concept for active loudspeaker systems with very low energy consumption*, J. Audio Eng. Soc., **45**, 7/8 (1997).
- [8] JOHANSEN M., NIELSEN K., *A review and comparison of digital PWM methods for digital pulse modulation amplifier (PMA)*, Proc. of the AES Convention, paper 5039, New York, September 24–27, 1999.
- [9] BRESCH E., PADGETT W. T., *TMS320C67-based design of a digital audio power amplifier introducing novel feedback strategy*, Rose-Hulman Institute of Technology, www.mathworks.com.
- [10] BERKHOUT M., *Integrated class D amplifier*, Proc. of the AES Convention, paper 5502, Munich, May 10–13, 2002.
- [11] VARONA J., *Power digital-to-analog using sigma-delta and pulse width modulations*, ECE University of Toronto, ECE1371 Analog Electronics II.
- [12] GERZON M. A., *Predistortion techniques for complex but predictable transmission systems*, J. Audio Eng. Soc., **20**, 6 (1972).
- [13] HAWKSFORD M. O. J., *Dynamic model-based linearization of quantized pulse-width modulation for applications in digital-to-analog conversion and digital power amplifier systems*, J. Audio Eng. Soc., **40**, 4 (1992).
- [14] CRAVEN P., *Toward the 24-bit DAC: novel noise-shaping topologies incorporating correction for the nonlinearity in a PWM output stage*, J. Audio Eng. Soc., **41**, 5 (1993).
- [15] HAWKSFORD M. O. J., *Linearization of multilevel, multiwidth digital PWM with applications in digital-to-analog conversion*, J. Audio Eng. Soc., **43**, 10 (1995).
- [16] KOSTRZEWA M., *Use of PCM-to-PWM signal conversion methods in digital audio amplifiers* [in Polish], Proc. of the 9-th Symposium – New Trends in Audio and Video, Warsaw, September 27–28, 2002.
- [17] YANG M., OH J-H., *Adaptive predistortion filter for linearization of digital PWM power amplifier using neural networks*, Proc. of the 113-th AES Convention, paper 5657, Los Angeles, October 5–8, 2002.
- [18] ANDERSON J. et al., *Second generation intelligent class D amplifier controller integrated circuit enables both low cost and high performance amplifier designs*, Proc. of the 120-th AES Convention, paper 6692, Paris, May 20–23, 2006.
- [19] TAURA K. et al., *Development of a digital amplifier for car use*, Proc. of the 115-th AES Convention, paper 5963, New York, October 10–13, 2003.
- [20] PERUZZI R. et al., *An efficient lo-power audio amplifier with power supply rails tracking the output by means of pulse width modulation*, Proc. of the 115-th AES Convention, paper 5920, New York, October 10–13, 2003.
- [21] TOL J. et al., *A digital class-D amplifier with power supply correction*, Proc. of the 121-st AES Convention, paper 6860, San Francisco, October 5–8, 2006.
- [22] ESSLINGER R., GRUHLER G., STEWART R. W., *Digital audio power amplifiers using sigma-delta modulation. Linearity problems in the class-D power stage*, Proc. of the 110-th AES Convention, paper 5400, Amsterdam, May 12–15, 2001.

-
- [23] ESSLINGER R., GRUHLER G., STEWART R. W., *Sigma-delta modulation in digital class-D power amplifiers: Methods for reducing the effective pulse transition rate*, Proc. of the 112-th AES Convention, paper 5634, Munich, May 10–13, 2002.
 - [24] GAALAAS E. *et al.*, *Integrated stereo sigma-delta class D amplifier*, Proc. of the 118-th AES Convention, paper 6452, Barcelona, May 28–31, 2005.
 - [25] MAGRATH A. J., SANDLER M. B., *Digital-domain dithering of sigma-delta modulators using bit flipping*, J. Audio Eng. Soc., **45**, 6 (1997).
 - [26] GABORIAU J., FEI X., WALBURGER E., *High performance PWM power audio amplifier*, Proc. of the 111-th AES Convention, paper 5428, New York, September 21–24, 2001.
 - [27] LOGAN B. F. Jr., *Click modulation*, AT&T Bell Lab. Tech., **63**, 3 (1984).
 - [28] KOSTRZEWA M., KULKA Z., *Time-domain performance investigation of the click modulation-based PWM for digital class-D audio power amplifiers*, Proc. of the IEEE Signal Processing '2005, Poznań, September 30, 2005.
 - [29] STREITENBERGER M., BRESCH H., MATHIS W., *A new concept for high performance class-D audio amplification*, Proc. of the 106-th AES Convention, paper 4941, Munich, May 8–11, 1999.
 - [30] STREITENBERGER M., MATHIS W., *A novel coding topology for digital class-D audio power amplifiers with very low pulse-repetition rate*, Proc. ESSCIRC, 2002.
 - [31] OLIVA A., PAOLINI E., ANG S., *A new audio file format for low-cost, high-fidelity, portable digital power amplifiers*, www.techonline.com, 2005.